AzureWave Technologies, Inc.

# AW-AM510

## IEEE 802.11 1X1 a/b/g/n Wireless LAN + Bluetooth 5.1 Combo 12 x 12 LGA Module

## Datasheet

**Rev. B**

**DF**

**For Standard**



FORM NO.: FR2-015_ A Responsible Department：WBU Expiry Date: Forever
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# Features

## WLAN

- Support 802.11 a/b/g/n
- Dual bands: 2.4 GHz and 5 GHz
- Single stream 802.11n with 20/40 MHz channels for 5G and 20 MHz only for 2.4G
- Up to MCS7 data rates (150 Mbps)
- Support 802.11mc for location
- Dynamic Rapid Channel Switching (DRCS) for simultaneous and power efficient operation in 2.4 GHz and 5 GHz bands
- Interface to coexist with 802.15.4, LTE, or other radios.
- Security: WPA3, WPA2, WPA2 and WPA mix mixed mode, WEP

## Bluetooth

- Full Bluetooth 5.1 features
- Long range - 4x coverage
- 2 Mbps data rate - 2x faster
- Connection/connectionless AoA
- Connection/connectionless AoD
- Improved advertisement capacity- enables more IoT services
- Audio interface: I2S and PCM
- Security: AES


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# Revision History

Document NO: R2-2510-DST-01

| Version | Revision Date | DCN NO. | Description | Initials | Approved |
|---|---|---|---|---|---|
| A | 2020/09/17 | DCN018312 | ● Draft version | Renton Tao | N.C Chen |
| B | 2021/04/19 | DCN021490 | ● Modify pin table<br>● Modify datasheet form<br>● Modify block diagram<br>● Modify spec. table | Roger Liu | N.C Chen |
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# 1. Introduction

## 1.1 Product Overview

**AzureWave Technologies, Inc.** introduces the IEEE 802.11a/b/g/n WLAN, BT, combo module – **AW-AM510.** With four advanced radio technologies integrated into a module, AW-AM510 provides the best and most convenient SMT process. The module is targeted to mobile devices including**,** Tablet PC, Portable Media Players (PMPs), Portable Navigation Devices (PNDs), Personal Digital Assistants (PDAs), Tracking Devices, Gaming Devices which need convenient SMT process, low power consumption.

By using AW-AM510, the customers can easily integrate the Wi-Fi, BT, by a combo module with the benefits of **high design flexibility, high success rate on SMT process, short development cycle, and quick time-to-market.**

Compliance with the IEEE 802.11a/b/g/n standard, the AW-AM510 uses **DSSS**, **OFDM**, **DBPSK**, **DQPSK**, **CCK** and **QAM** baseband modulation technologies. A high level of integration and full implementation of the power management functions specified in the IEEE 802.11 standard minimize the system power requirements by using AW-AM510.

The AW-AM510 supports standard interface **SDIO3.0 for WLAN**, **SDIO3.0 and UART, for BT**. AW-AM510 is suitable for multiple mobile processors for different applications. With the combo functions and the good performance, the AW-AM510 is the best solution for the consumer electronics and the tablet PC.



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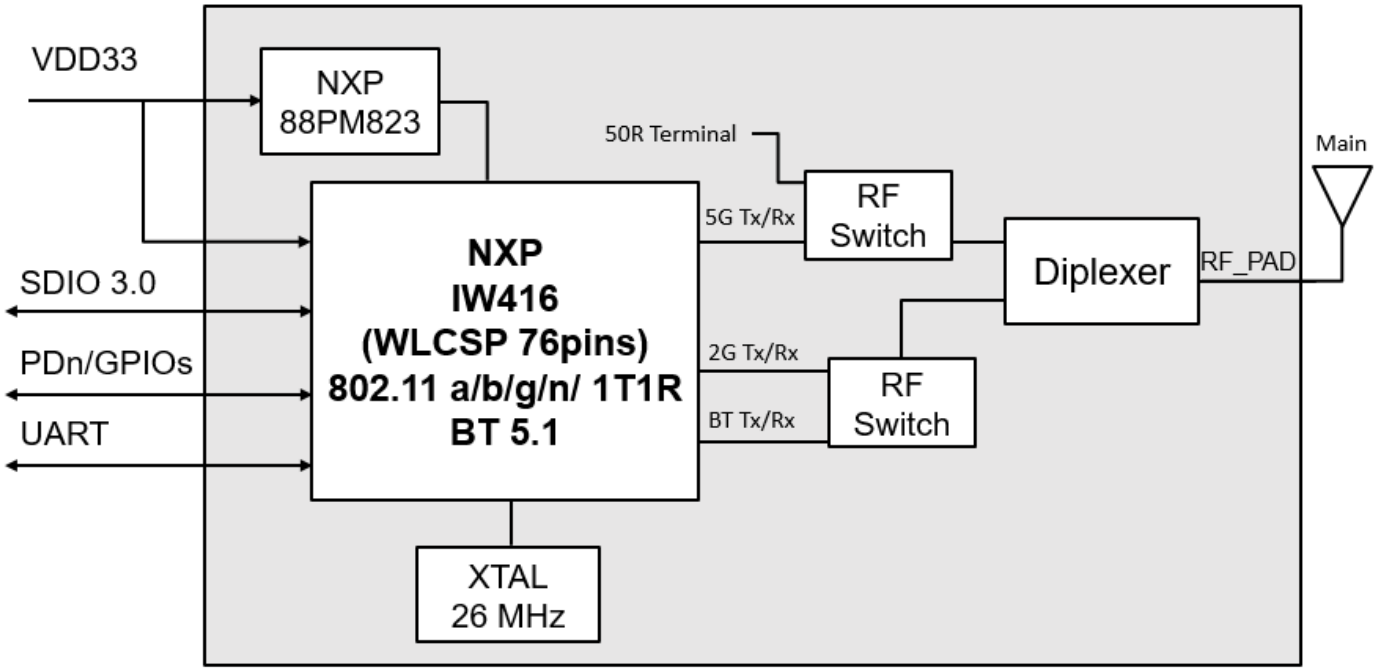
## 1.2 Block Diagram

A simplified block diagram of the AW-AM510 module is depicted in the figure below.




**AW-AM510 Block Diagram**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## 1.3 Specifications Table

### 1.3.1 General

| Features | Description |
|---|---|
| **Product Description** | IEEE 802.11 a/b/g/n Wi-Fi with Bluetooth 5.1 Combo Module |
| **Major Chipset** | NXP IW416 WLCSP (76p) |
| **Host Interface** | WiFi + BT<br>● SDIO + UART<br>● SDIO + SDIO |
| **Dimension** | 12 mm X 12 mm x 2 mm(Max) |
| **Form Factor** | LGA module, 44 pins |
| **Antenna** | ANT(Main)：WiFi/Bluetooth → TX/RX |
| **Weight** | 0.2g |

### 1.3.2 WLAN

| Features | Description |
|---|---|
| **WLAN Standard** | IEEE 802.11 a/b/g/n Wi-Fi with Bluetooth 5.1 Combo Module |
| **WLAN VID/PID** | NA |
| **WLAN SVID/SPID** | NA |
| **Frequency Rage** | 2.4 GHz ISM Bands 2.412-2.472 GHz<br>5.15-5.25 GHz (FCC UNII-low band) for US/Canada and Europe<br>5.25-5.35 GHz (FCC UNII-middle band) for US/Canada and Europe<br>5.47-5.725 GHz for Europe<br>5.725-5.825 GHz (FCC UNII-high band) for US/Canada |
| **Modulation** | DSSS, OFDM, DBPSK, DQPSK, CCK, 16-QAM, 64-QAM |


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<table>
<tr><td>Number of Channels</td><td>2.4GHz:<br>■ USA, NORTH AMERICA, Canada and Taiwan - 1 ~ 11<br>■ China, Australia, Most European Countries - 1 ~ 13<br>■ Japan, 1 ~ 13<br><br>5GHz:<br>■ USA, Canada, Most European Countries - 36,40,44,48,52,56,60,64,100,104,108,112,116,120,124,128,132,136,140,149,153,157,161,165<br>■ Japan - 36,40,44,48,52,56,60,64,100,104,108,112,116,120,124,128,132,136,140<br>■ China - 36,40,44,48,52,56,60,64, 149,153,157,161,165</td></tr>
<tr><td>Output Power<br>(Board Level Limit)*</td><td>2.4G
<table>
<tr><th></th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>11b (11Mbps)<br>@EVM<35%</td><td>15.5</td><td>17</td><td>18.5</td><td>dBm</td></tr>
<tr><td>11g (54Mbps)<br>@EVM≦-27 dB</td><td>14.5</td><td>16</td><td>17.5</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7)<br>@EVM≦-28 dB</td><td>12.5</td><td>14</td><td>15.5</td><td>dBm</td></tr>
</table>
5G
<table>
<tr><th></th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>11a (54Mbps)<br>@EVM≦-27 dB</td><td>14</td><td>16</td><td>18</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7)<br>@EVM≦-28 dB</td><td>13</td><td>15</td><td>17</td><td>dBm</td></tr>
<tr><td>11n (HT40 MCS7)<br>@EVM≦-28 dB</td><td>12</td><td>14</td><td>16</td><td>dBm</td></tr>
</table></td></tr>
</table>


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<table>
<tr><td>Receiver Sensitivity</td><td>
2.4G
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>11b (11Mbps)</td><td>-</td><td>-86</td><td>-83</td><td>dBm</td></tr>
<tr><td>11g (54Mbps)</td><td>-</td><td>-73</td><td>-70</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7)</td><td>-</td><td>-69</td><td>-66</td><td>dBm</td></tr>
</table>
5G
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>11a (54Mbps)</td><td>-</td><td>-71</td><td>-68</td><td>dBm</td></tr>
<tr><td>11n (HT20 MCS7)</td><td>-</td><td>-68</td><td>-65</td><td>dBm</td></tr>
<tr><td>11n (HT40 MCS7)</td><td>-</td><td>-66</td><td>-63</td><td>dBm</td></tr>
</table>
</td></tr>
<tr><td>Data Rate</td><td>WLAN:<br>802.11b : 1, 2, 5.5, 11Mbps<br>802.11a/g : 6, 9, 12, 18, 24, 36, 48, 54Mbps<br>802.11n : Maximum data rates up to 72 Mbps (20 MHz channel), 150 Mbps (40 MHz channel)</td></tr>
<tr><td>Security</td><td>■ WiFi: WPA3, WPA2, WPA2 and WPA mixed mode, WEP<br>■ BT: AES</td></tr>
</table>

* If you have any certification questions about output power please contact FAE directly.

## 1.3.3 Bluetooth

<table>
<tr><th>Features</th><th>Description</th></tr>
<tr><td>Bluetooth Standard</td><td>Full Bluetooth 5.1 features</td></tr>
<tr><td>Frequency Rage</td><td>2402MHz~2483MHz</td></tr>
<tr><td>Modulation</td><td>Header GFSK<br>Payload 2M: π/4-DQPSK<br>Payload 3M: 8DPSK</td></tr>
<tr><td>Output Power</td><td>
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>BDR</td><td>0</td><td>2</td><td>4</td><td>dBm</td></tr>
<tr><td>EDR</td><td>0</td><td>2</td><td>4</td><td>dBm</td></tr>
<tr><td>Low Energy</td><td>0</td><td>2</td><td>4</td><td>dBm</td></tr>
</table>
</td></tr>
</table>


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<table>
<tr><td>Receiver Sensitivity</td><td>BT Sensitivity (BER<0.1%)
<table>
<tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr>
<tr><td>BDR(DH1)</td><td>-</td><td>-83</td><td>-80</td><td>dBm</td></tr>
<tr><td>EDR(2DH5)</td><td>-</td><td>-88</td><td>-85</td><td>dBm</td></tr>
<tr><td>EDR(3DH5)</td><td>-</td><td>-83</td><td>-80</td><td>dBm</td></tr>
<tr><td>Low Energy</td><td>-</td><td>-96</td><td>-93</td><td>dBm</td></tr>
</table></td></tr>
</table>

### 1.3.4 Operating Conditions

| Features | Description |
|---|---|
| Operating Conditions | |
| **Voltage** | 3.3V +-5% |
| **Operating Temperature** | 0 ºC to +70 ºC |
| **Operating Humidity** | Less than 85% R.H. |
| **Storage Temperature** | -40 ºC to +85 ºC |
| **Storage Humidity** | Less than 60% R.H. |
| **ESD Protection** | |
| **Human Body Model** | TBD |
| **Changed Device Model** | TBD |


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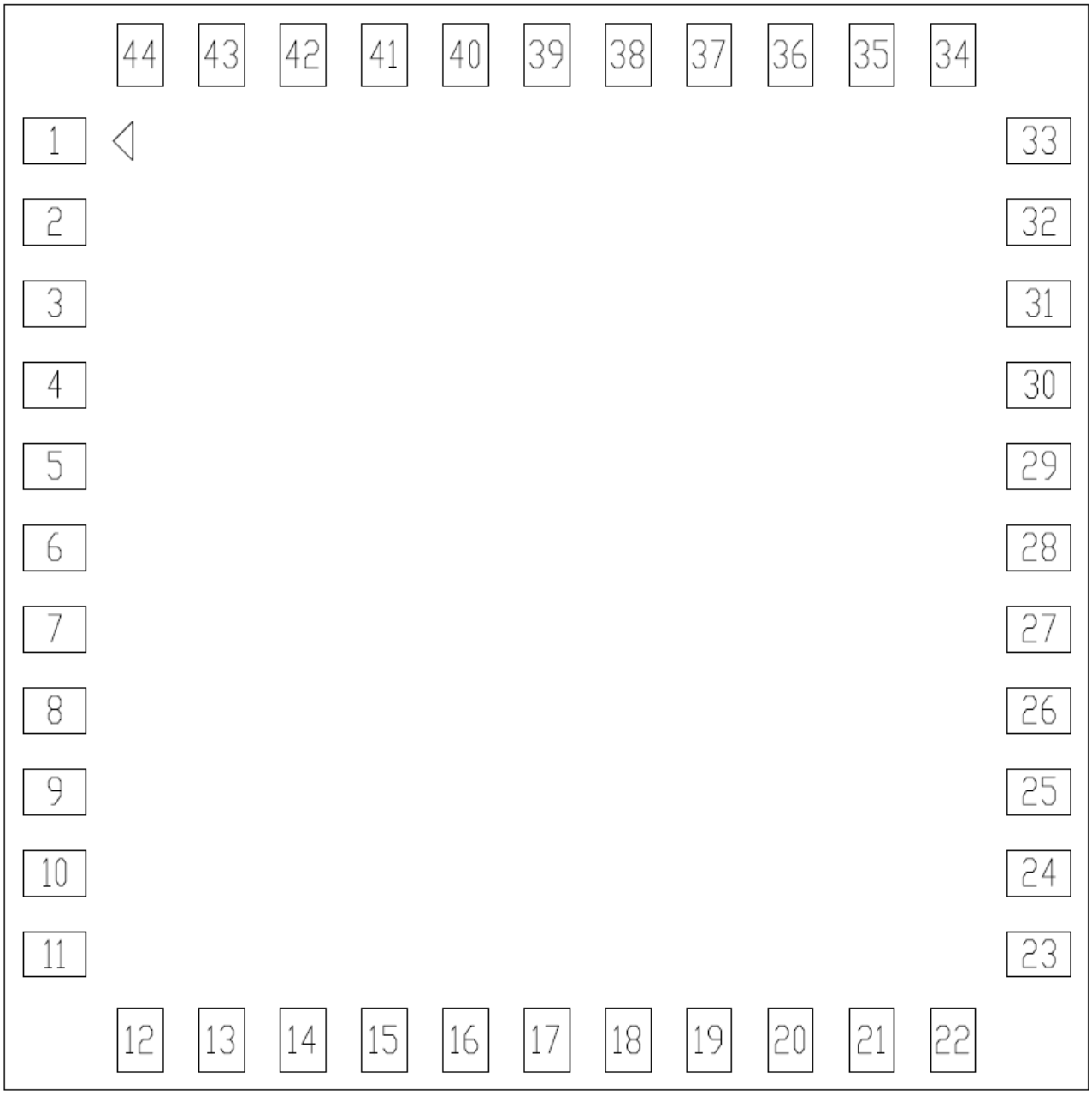
# 2. Pin Definition

## 2.1 Pin Map




AW-AM510 Pin Map (top view)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## 2.2 Pin Table

| Pin No | Definition | Basic Description | Voltage | Type |
|---|---|---|---|---|
| 1 | GND1 | Ground | --- | --- |
| 2 | RF_ANT | Option for RF I/O pin out | 1.8V | I/O |
| 3 | GND3 | Ground | --- | --- |
| 4 | NC4 | Floating Pin, No connect to anything. | --- | Floating |
| 5 | NC5 | Floating Pin, No connect to anything. | --- | Floating |
| 6 | HOST_WAKE_ BT | GPIO Mode : GPIO[12].<br>BT Device Wake | VDDIO | I |
| 7 | BT_WAKE_HOST | GPIO Mode : GPIO[0].<br>BT Host Wake | VDDIO | O |
| 8 | NC8 | Floating Pin, No connect to anything. | --- | Floating |
| 9 | VBAT | 3.3V power voltage source input | 3.3V | P |
| 10 | NC10 | Floating Pin, No connect to anything. | --- | Floating |
| 11 | NC11 | Floating Pin, No connect to anything. | --- | Floating |
| 12 | PDn | Full Power-down (input) (active low)<br>0 = full power-down mode<br>1 = normal mode | VDDIO | I |
| 13 | WL_WAKE_HOST | GPIO Mode : GPIO[1].<br>WL Host Wake | VDDIO | I/O |
| 14 | SDIO_DATA2 | SDIO Data line Bit[2] | VDDIO | I/O |
| 15 | SDIO_DATA3 | SDIO Data line Bit[3] | VDDIO | I/O |
| 16 | SDIO_CMD | SDIO Command | VDDIO | I/O |
| 17 | SDIO_CLK | SDIO Clock input | VDDIO | I |
| 18 | SDIO_DATA0 | SDIO Data line Bit[0] | VDDIO | I/O |
| 19 | SDIO_DATA1 | SDIO Data line Bit[1] | VDDIO | I/O |
| 20 | GND20 | Ground | --- | --- |
| 21 | NC21 | Floating Pin, No connect to anything. | --- | Floating |
| 22 | VDDIO | 1.8V/3.3V Digital I/O Power Supply | 1.8V/3.3V | P |
| 23 | NC23 | Floating Pin, No connect to anything. | --- | Floating |
| 24 | SUSCLK_IN | External Low Power Clock input(32.768KHz) (optional) | VDDIO | I |
| 25 | BT_PCM_OUT | PCM Data output | VDDIO | I/O |
| 26 | BT_PCM_CLK | PCM Clock | VDDIO | I/O |
| 27 | BT_PCM_IN | PCM data input | VDDIO | I/O |
| 28 | BT_PCM_SYNC | PCM sync signal | VDDIO | I/O |
| 29 | GPIO[3] | GPIO[3] /JTAG_TDO | VDDIO | I/O |
| 30 | GPIO[2] | GPIO[2] /JTAG_TDI | VDDIO | I/O |
| 31 | GND31 | Ground | --- | --- |
| 32 | NC32 | Floating Pin, No connect to anything. | --- | Floating |
| 33 | GND33 | Ground | --- | --- |
| 34 | GPIO[15] | Host-to-BT reset / GPIO[15] / JTAG_TMS | VDDIO | I |
| 35 | NC35 | Floating Pin, No connect to anything. | --- | Floating |


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| | | | | |
|---|---|---|---|---|
| 36 | GND36 | Ground | --- | --- |
| 37 | HOST_WAKE_WL | Host-to-WLAN wake/GPIO[14]/JTAG_TCK | VDDIO | I/O |
| 38 | MWS_SOUT | WCI-2 MWS coexistence serial transport interface(TX) | VDDIO | I/O |
| 39 | MWS_SIN | WCI-2 MWS coexistence serial transport interface(RX) | VDDIO | I/O |
| 40 | GPIO[13] | GPIO Mode : GPIO[13].<br>Host-to-Wi-Fi reset recovery | VDDIO | I/O |
| 41 | UART_RTS_N | UART_RTSn (active low) | VDDIO | O |
| 42 | UART_TXD | UART_SOUT | VDDIO | O |
| 43 | UART_RXD | UART_SIN | VDDIO | I |
| 44 | UART_CTS_N | UART_CTSn(active low) | VDDIO | I |

# 3. Electrical Characteristics

## 3.1 Absolute Maximum Ratings

| Symbol | Parameter | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| VBAT | DC supply for the 3.3V input | - | 3.3 | 3.96 | V |
| VDDIO | I/O power supply | - | 3.3 | 4.0 | V |
| | | - | 1.8 | 2.2 | |

## 3.2 Recommended Operating Conditions

| Symbol | Parameter | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| VBAT | DC supply for the 3.3V input | 3.14 | 3.3 | 3.46 | V |
| VDDIO | 1.8V/3.3V digital I/O power supply | 2.97 | 3.3 | 3.47 | V |
| | | 1.62 | 1.8 | 1.98 | |

## 3.3 Digital IO Pin DC Characteristics

### 3.3.1 1.8V Operation (VDDIO)

| Symbol | Parameter | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| $V_{IH}$ | Input high voltage | 0.7*VIO | - | VIO+0.4 | V |
| $V_{IL}$ | Input low voltage | -0.4 | - | 0.3*VIO | |
| $V_{OH}$ | Output high voltage | VIO-0.4 | - | - | |


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| | | | | | |
|---|---|---|---|---|---|
| $V_{OL}$ | Output low voltage | - | - | 0.4 | |
| $V_{HYS}$ | Input Hysteresis | 100 | | | mV |

### 3.3.2 3.3V Operation (VDDIO)

| Symbol | Parameter | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| $V_{IH}$ | Input high voltage | 0.7*VIO | - | VIO+0.4 | V |
| $V_{IL}$ | Input low voltage | -0.4 | - | 0.3*VIO | |
| $V_{OH}$ | Output High Voltage | VIO-0.4 | - | - | |
| $V_{OL}$ | Output Low Voltage | - | - | 0.4 | |
| $V_{HYS}$ | Input Hysteresis | 100 | | | mV |


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## 3.4 Host Interface

### 3.4.1 SDIO Interface

The AW-AM510 supports a SDIO device interface that conforms to the industry SDIO Full-Speed card specification and allows a host controller using the SDIO bus protocol to access the Wireless SoC device.

The AW-AM510 acts as the device on the SDIO bus. The host unit can access registers of the SDIO interface directly and can access shared memory in the device through the use of BARs and a DMA engine.

- Support SDIO 3.0 Standard.
- On-chip memory used for CIS.
- Supports 4-bit SDIO and 1-bit SDIO transfer modes.
- Special interrupt register for information exchange.
- Allows card to interrupt host.

**SDIO Interface Signals**

| AW-AM510 SDIO Pin Name | Type | Description |
|---|---|---|
| SDIO_CLK | I | SDIO 4-bit mode: Clock<br>SDIO 1-bit mode: Clock |
| SDIO_CMD | I/O | SDIO 4-bit mode: Command line<br>SDIO 1-bit mode: Command line |
| SDIO_DATA3 | I/O | SDIO 4-bit mode: Data line Bit[3]<br>SDIO 1-bit mode: Not used |
| SDIO_DATA2 | I/O | SDIO 4-bit mode: Data line Bit[2] or Read Wait (optional)<br>SDIO 1-bit mode: Read Wait (optional) |
| SDIO_DATA1 | I/O | SDIO 4-bit mode: Data line Bit[1]<br>SDIO 1-bit mode: Interrupt |
| SDIO_DATA0 | I/O | SDIO 4-bit mode: Data line Bit[0]<br>SDIO 1-bit mode: Data line |


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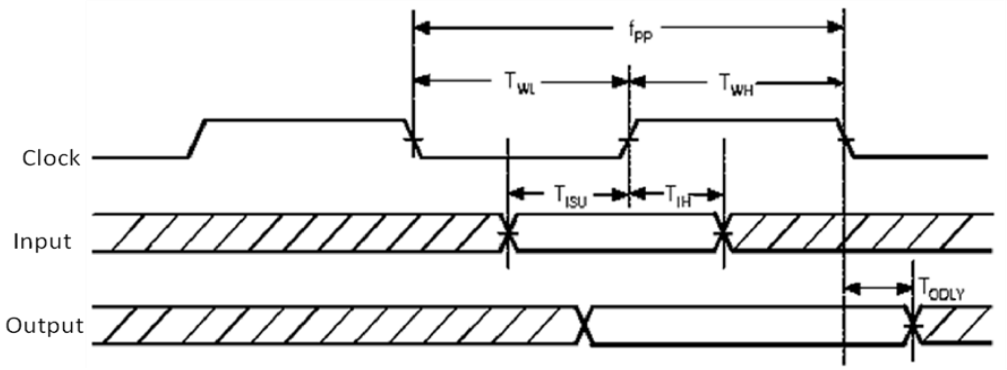
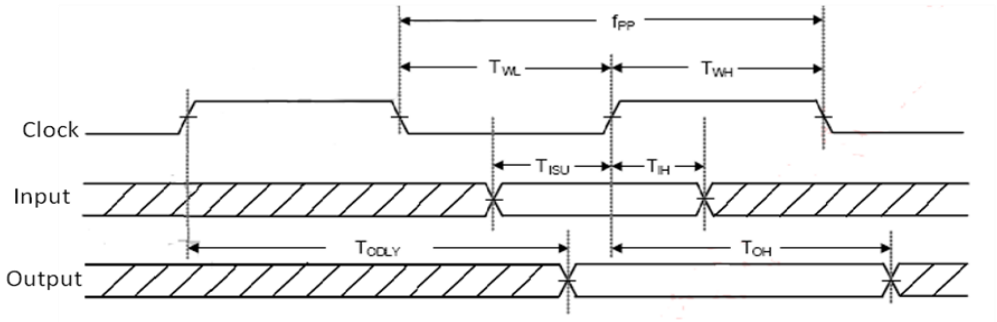
## 3.4.2 SDIO Protocol Timing

### 3.4.2.1 Default Speed, High-Speed Modes (3.3V)




SDIO protocol timing Diagram - Default mode. (3.3V)




SDIO protocol timing Diagram - High Speed mode. (3.3V)

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| fpp | CLK Frequency | Normal | 0 | -- | 25 | MHz |
| | | High Speed | 0 | -- | 50 | MHz |
| $T_{WH}$ | CLK High Time | Normal | 10 | -- | -- | ns |
| | | High Speed | 7 | -- | -- | ns |
| $T_{WL}$ | CLK Low Time | Normal | 10 | -- | -- | ns |
| | | High Speed | 7 | -- | -- | ns |
| $T_{ISU}$ | Input Setup Time | Normal | 5 | -- | -- | ns |
| | | High Speed | 6 | -- | -- | ns |
| $T_{IH}$ | Input Hold Time | Normal | 5 | -- | -- | ns |
| | | High Speed | 2 | -- | -- | ns |
| $T_{ODLY}$ | Output Delay Time | Normal | -- | -- | 14 | ns |
| | CL ≦ 40pF (1 card) | High Speed | -- | -- | 14 | ns |
| $T_{OH}$ | Output Hold Time | High Speed | 2.5 | -- | -- | ns |

SDIO Timing Data – Default Speed / High-Speed modes. (3.3V)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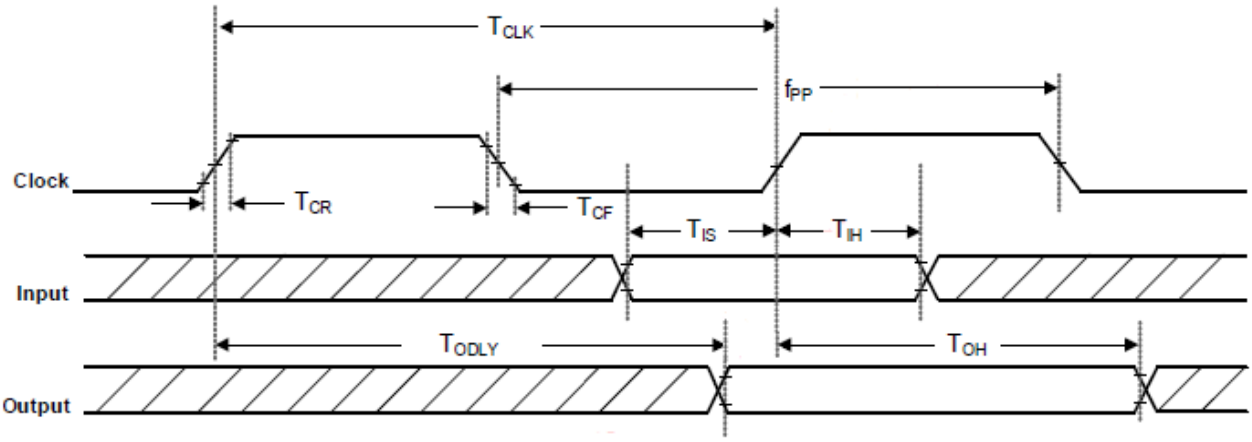
### 3.4.2.2 SDR12, SDR25, SDR50 Modes (up to 100MHz) (1.8V)




SDIO Protocol Timing Diagram - SDR12, SDR25, SDR50 Modes (up to 100 MHz)(1.8V)

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $F_{pp}$ | CLK Frequency | SDR12/25/50 | 25 | - | 100 | MHz |
| $T_{CLK}$ | Clock Time | SDR12/25/50 | 10 | - | 40 | ns |
| $T_{IS}$ | Input Setup Time | SDR12/25/50 | 3 | - | - | ns |
| $T_{IH}$ | Input Hold Time | SDR12/25/50 | 0.8 | - | - | ns |
| $T_{CR}$ ,$T_{CF}$ | Rise time, fail time<br>TCR ,TCF <2ns(max) at 100MHz<br>CCARD =10pF | SDR12/25/50 | - | - | 0.2*$T_{CLK}$ | ns |
| $T_{ODLY}$ | Output Delay Time<br>CL ≦ 30pF | SDR12/25/50 | - | - | 7.5 | ns |
| $T_{OH}$ | Output Hold Time<br>CL =15pF | SDR12/25/50 | 1.5 | - | - | ns |

SDIO Timing Data - SDR12/25/50 modes. (1.8V)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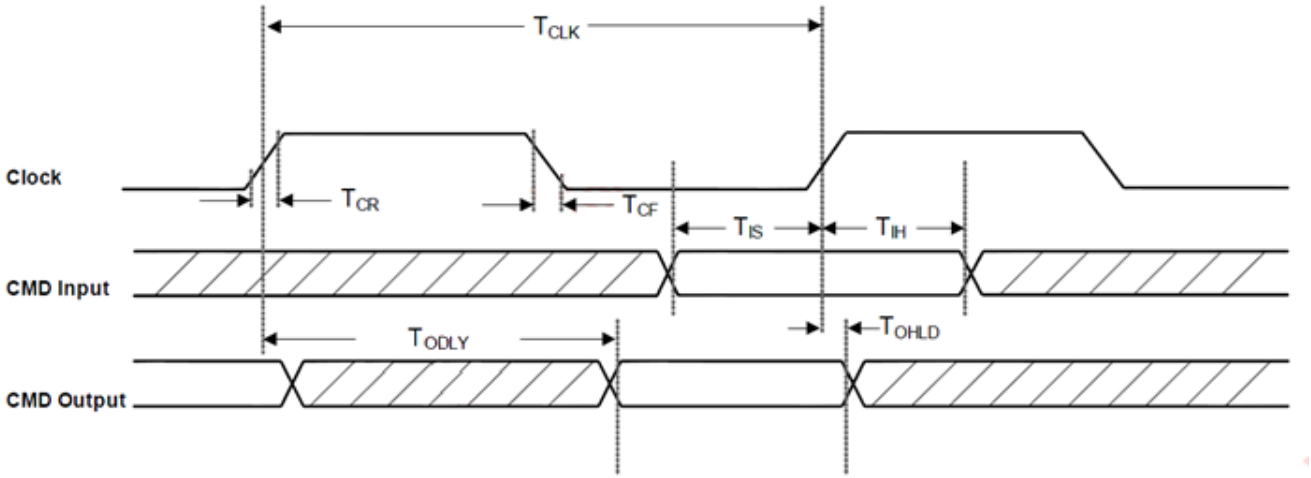
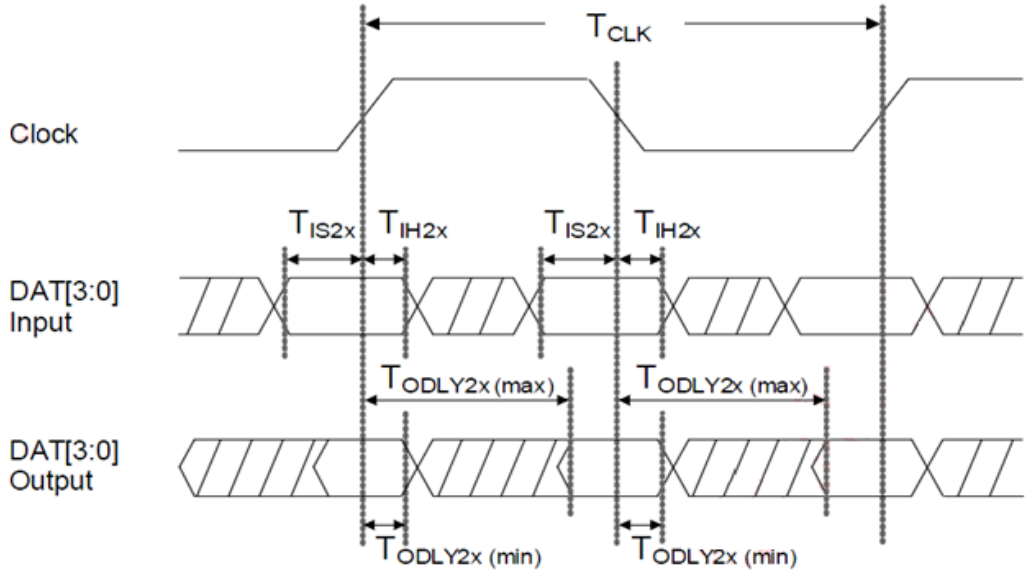
### 3.4.2.3 DDR50 Mode (50MHz) (1.8V)




SDIO CMD Timing Diagram - DDR50 Mode (50 MHz)




SDIO DAT[3:0] Timing Diagram - DDR50 Mode[1] (50 MHz)

[1] In DDR50 mode, DAT[3:0] lines are sampled on both edges of the clock (not applicable for CMD line).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| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Clock | | | | | | |
| $T_{CLK}$ | Clock time | DDR50 | 20 | - | - | ns |
| $T_{CR}$, $T_{CF}$ | Rise time, fall time | DDR50 | - | - | 0.2*$T_{CLK}$ | Ns |
| Clock Duty | | DDR50 | 45 | - | 55 | % |
| CMD Input | | | | | | |
| $T_{IS}$ | Input setup time | DDR50 | 6 | - | - | ns |
| $T_{IH}$ | Input hold time | DDR50 | 0.8 | - | - | ns |
| CMD Output | | | | | | |
| $T_{ODLY}$ | Output delay time during data transfer mode | DDR50 | - | - | 13.7 | ns |
| $T_{OHLD}$ | Output hold time | DDR50 | 1.5 | - | - | ns |
| DAT [3:0] Input | | | | | | |
| $T_{IS2X}$ | Input setup time | DDR50 | 3 | - | - | ns |
| $T_{IH2X}$ | Input hold time | DDR50 | 0.8 | - | - | ns |
| DAT [3:0] Output | | | | | | |
| $T_{ODLY2X(max)}$ | Output delay time during data transfer mode | DDR50 | - | - | 7 | ns |
| $T_{ODLY2X(min)}$ | Output hold time | DDR50 | 1.5 | - | - | ns |

SDIO Timing Data - DDR50 Mode (50MHz)


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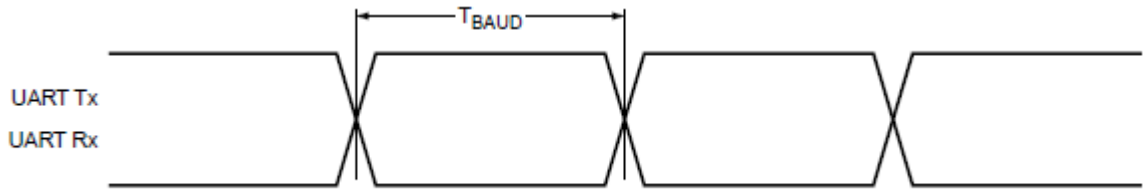
### 3.4.3.High-Speed UART Interface

The AW-AM510 supports a high-speed Universal Asynchronous Receiver/Transmitter (UART) interface, compliant to the industry standard 16550 specification. High-speed baud rates are supported to provide the physical transport between the device and the host for exchanging Bluetooth data.




| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $T_{BAUD}$ | Baud rate | 26MHz or 40MHz input clock | 250 | - | - | ns |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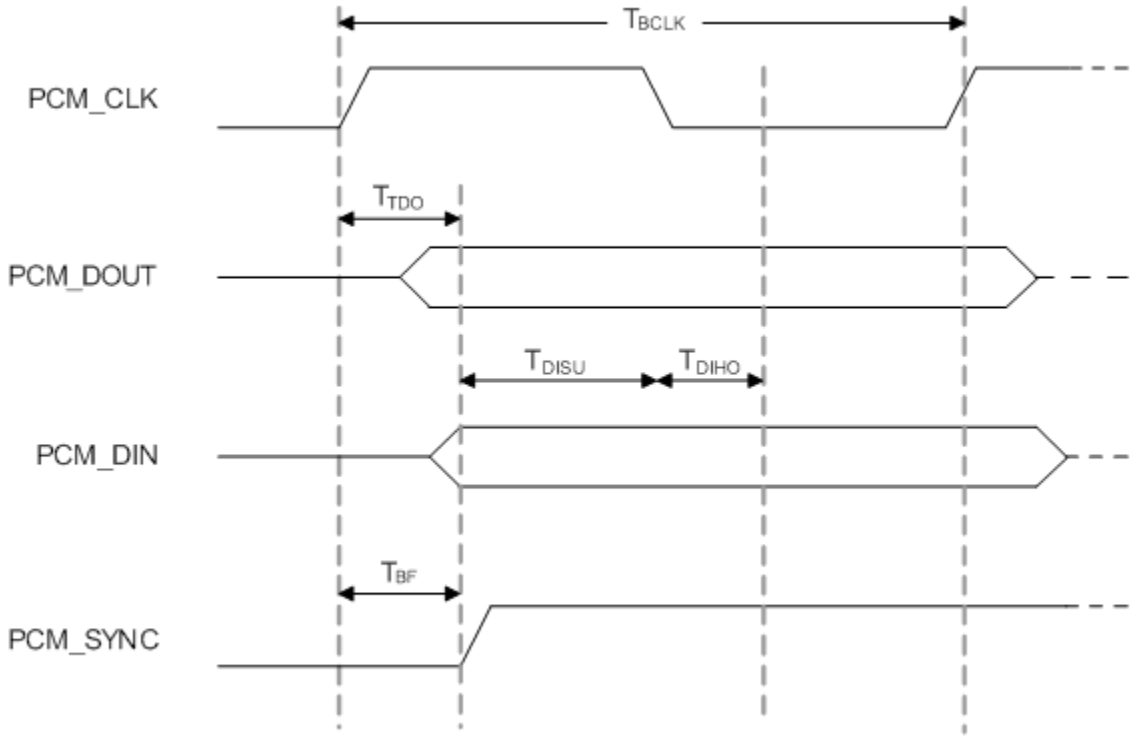
### 3.4.4 PCM Interface

#### 3.4.4.1 PCM Timing Specification – Master Mode




| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $F_{BCLK}$ | -- | -- | -- | 2/2.048 | -- | MHz |
| Duty $Cycle_{BCLK}$ | -- | -- | 0.4 | 0.5 | 0.6 | -- |
| $T_{BCLK\ rise/fall}$ | -- | -- | -- | 3 | -- | ns |
| $T_{DO}$ | -- | -- | -- | -- | 15 | ns |
| $T_{DISU}$ | -- | -- | 20 | -- | -- | ns |
| $T_{DIHO}$ | -- | -- | 15 | -- | -- | ns |
| $T_{BF}$ | -- | -- | -- | -- | 15 | ns |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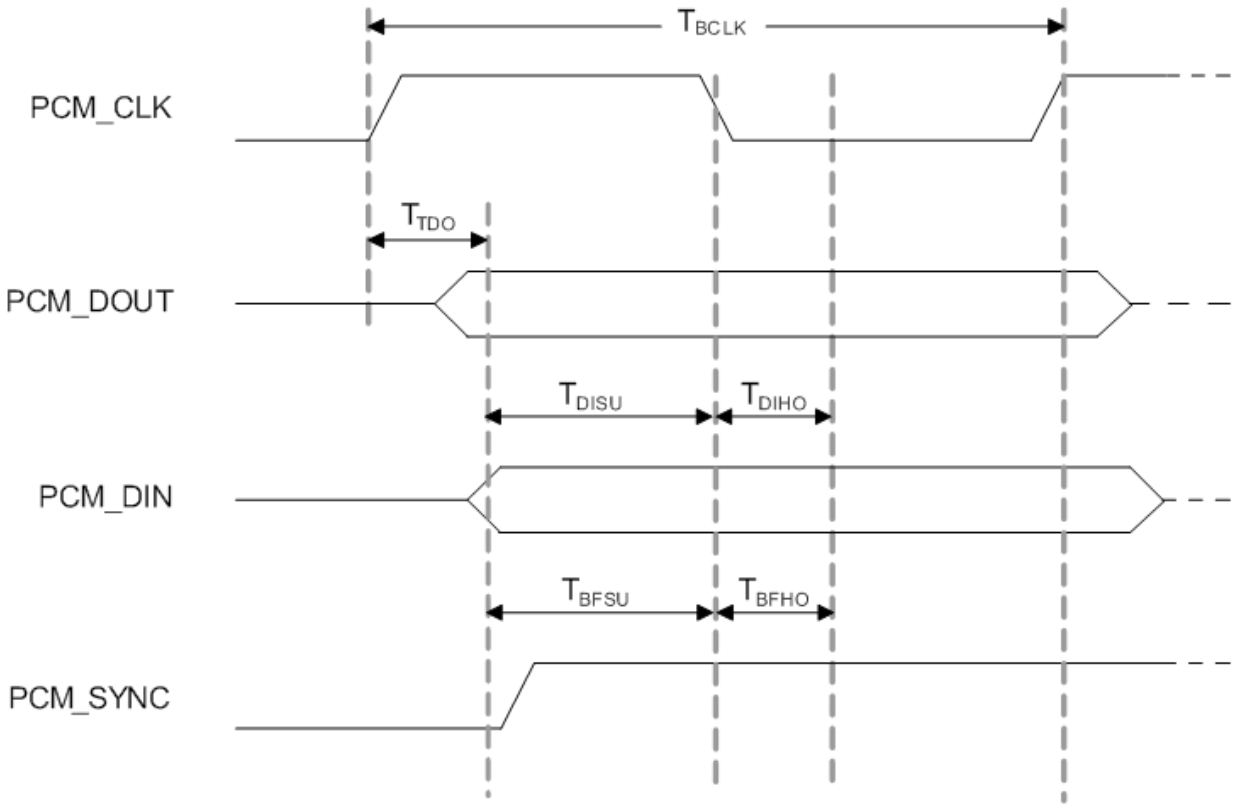
### 3.4.4.2 PCM Timing Specification – Slave Mode




| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $F_{BCLK}$ | -- | -- | -- | 2/2.048 | -- | MHz |
| Duty $Cycle_{BCLK}$ | -- | -- | 0.4 | 0.5 | 0.6 | -- |
| $T_{BCLK\ rise/fall}$ | -- | -- | -- | 3 | -- | ns |
| $T_{DO}$ | -- | -- | -- | -- | 30 | ns |
| $T_{DISU}$ | -- | -- | 15 | -- | -- | ns |
| $T_{DIHO}$ | -- | -- | 10 | -- | -- | ns |
| $T_{BFSU}$ | -- | -- | 15 | -- | -- | ns |
| $T_{BFHO}$ | | | 10 | | -- | ns |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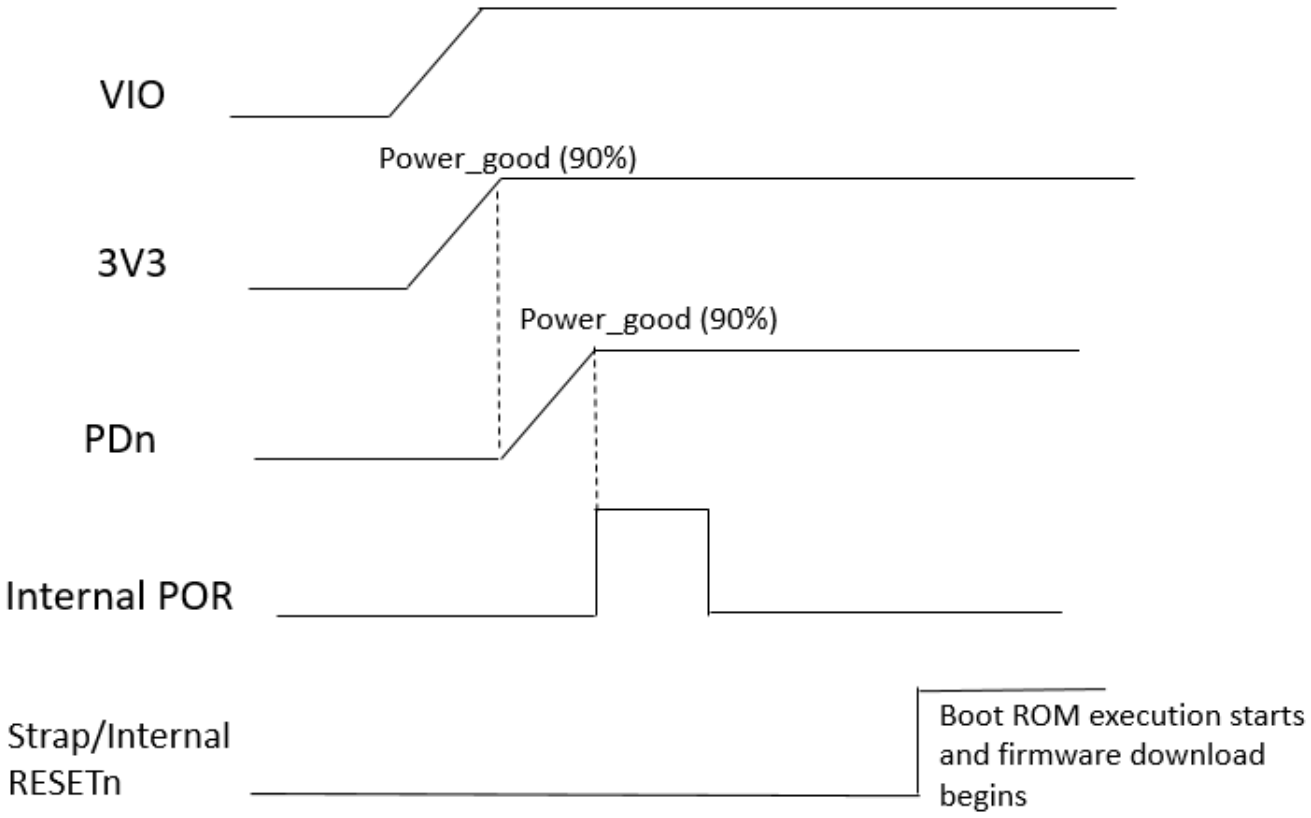
## 3.5 Timing Sequence

AW-AM510 power up timing sequence.





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## 3.6 Power Consumption*

### 3.6.1 WLAN

TBD

### 3.6.2 Bluetooth

TBD





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## 3.7 Sleep Clock(Optional)

An external crystal is used for generating all radio frequencies and normal operation clocking. As an alternative, an external frequency reference driven by a temperature-compensated crystal oscillator (TCXO) signal may be used. No software settings are required to differentiate between the two. In addition, a low-power oscillator (LPO) is provided for lower power mode timing.

## External 32.768KHz Low-Power Oscillator

| Symbol | Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| CLK | Clock frequency range/ accuracy<br>■ CMOS input clock signal type<br>■ ±250 ppm (initial, aging, temperature) | - | 32.768 | - | kHz |
| PN | Phase noise requirement (@ 100KHz) | - | -125 | - | dBc/Hz |
| $J_C$ | Cycle jitter | - | 1.5 | - | ns (RMS) |
| SR | Slew rate limit (10-90%) | - | - | 100 | ns |
| DC | Duty cycle tolerance | 20 | - | 80 | % |



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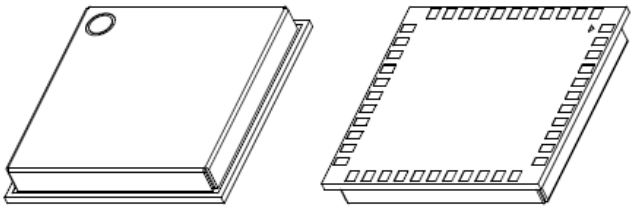
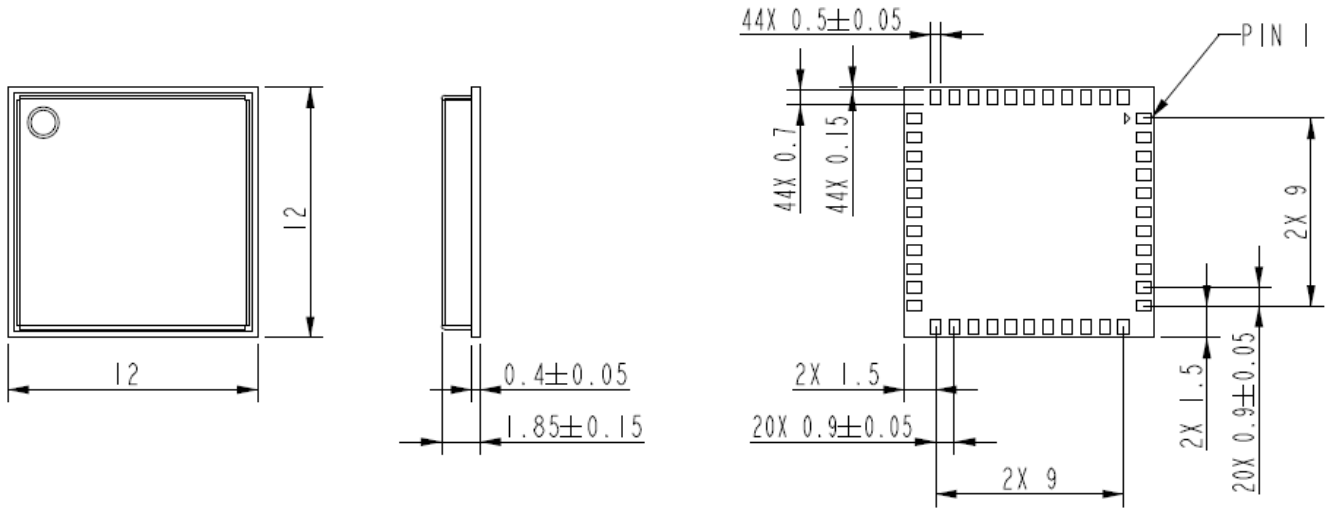
# 4. Mechanical Information

## 4.1 Mechanical Drawing






TOLERANCE UNLESS OTHERWISE SPECIFIED:±0.1mm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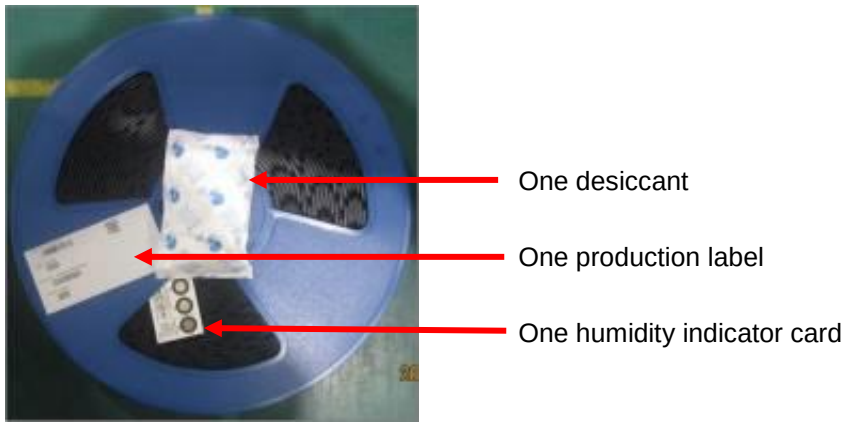
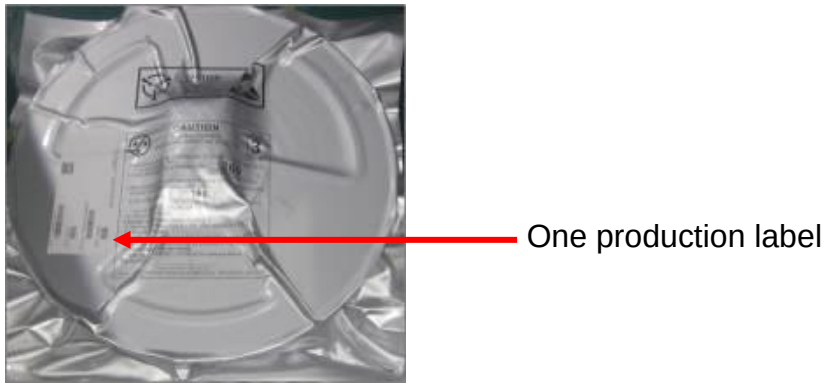
# 5. Packing Information

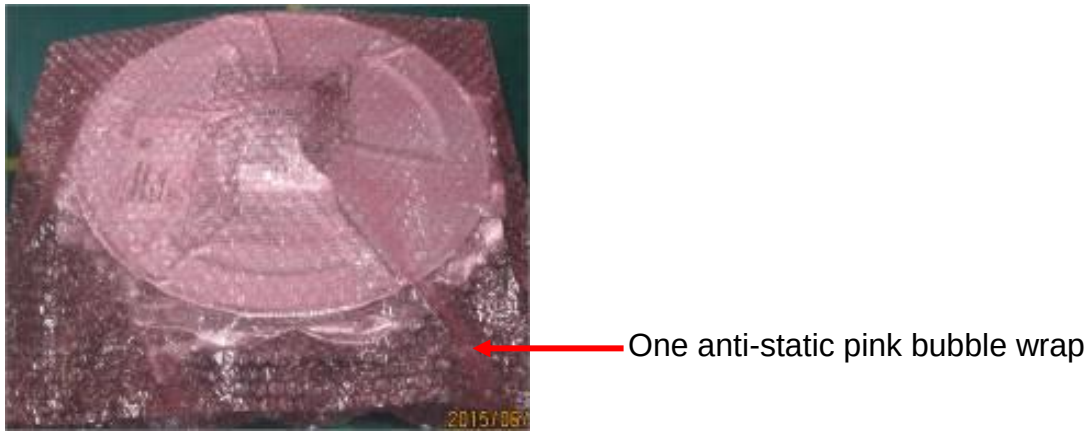
1. One reel can pack 1,500pcs 12x12 LGA modules
2. One production label is pasted on the reel, one desiccant and one humidity indicator card are put on the reel




3. One reel is put into the anti-static moisture barrier bag, and then one label is pasted on the bag




4. A bag is put into the anti-static pink bubble wrap





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5. A bubble wrap is put into the inner box and then one label is pasted on the inner box

One production label

6. 5 inner boxes could be put into one carton

7. Sealing the carton by AzureWave tape

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8. One carton label and one box label are pasted on the carton. If one carton is not full, one balance label pasted on the carton

One carton label
出貨標籤

One box label
箱號標籤

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